

**HIGH SPEED ADDER DESIGN  
FOR A MULTIPLY-ADD BASED FLOATING POINT UNIT**

ABSTRACT

5       An apparatus and computer program product are provided for  
improving a high-speed adder for Floating-Point Units (FPU) in a  
given computer system. The improved adder utilizes a compound  
incrementer, a compound adder, a carry network, an adder  
control/selector, and series of multiplexers (muxes). The carry  
10 network performs the end-around-carry function simultaneously to  
and independent of other required functions optimizing the  
functioning of the adder. Also, the use of a minimum number of  
muxes is also utilized to reduce mux delays.